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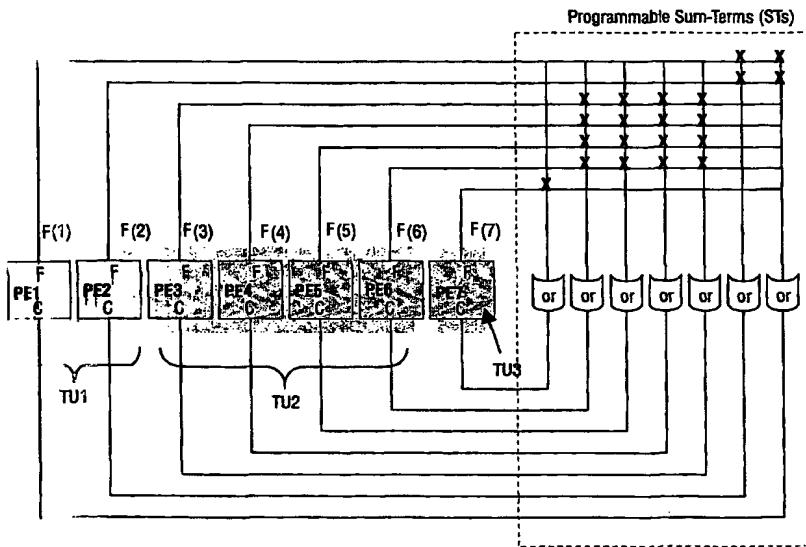
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[Continued on next page]

(54) Title: PROCESSING SYSTEM



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(57) Abstract: A processing system according to the invention comprises a plurality of processing elements (PE1,...,PE7). The processing elements comprise a controller and computation means. The plurality of processing elements is dynamically reconfigurable as mutually independently operating task units (TU1, TU2, TU3), which task units comprise one processing element (PE7) or a cluster of two or more processing elements (PE3, PE4, PE5, PE6). The processing elements within a cluster are arranged to execute instructions under a common thread of program control. In this way the processing system is capable of using the same sub-set of data-path elements to exploit instruction level parallelism or task level parallelism or a combination thereof, dependent on the application.



SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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B. FIELDS SEARCHED

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EPO-Internal, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 00/33186 A (SUN MICROSYSTEMS, INC) 8 June 2000 (2000-06-08) page 3, line 1 - page 4, line 22 page 7, line 7 - page 9, line 1; figure 3	1,5,6, 24,29
X	KECKLER S W ET AL: "Processor Coupling: Integrating Compile Time and Runtime Scheduling for Parallelism" ACM, 19 May 1992 (1992-05-19), pages 202-213, XP010324964 page 202, right-hand column, line 10 - line 36 page 203, left-hand column, line 14 - page 204, right-hand column, line 30; figures 2,3	1,2,29

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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